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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,371	06/13/2005	Santanu Dutta	US02 0563 US	6034

65913 7590 04/17/2008

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EXAMINER	
PARIKH, KALPIT	

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
04/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,371	DUTTA, SANTANU	
	Examiner	Art Unit	
	KALPIT PARIKH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 30, 2007 has been entered.

Examiner notes claims 5, 10 and 15 have been cancelled, however applicants' have not removed the text of the cancelled claim. 37 CFR 1.121 (c)(4) stipulates: "No claim text shall be presented for any claim in the claim listing with the status of "canceled" or "not entered." Examiner requests Applicants' remove the text of the cancelled claims in the next reply to comply with 37 CFR 1.121.

I. APPLICATION INFORMATION

The instant application having Application No. 10538371 has a total of 13 claims pending in the application; there are 3 independent claims and 10 dependent claims, all of which are ready for examination by the examiner.

II. REJECTIONS NOT BASED ON PRIOR ART

Claim Objections

Claims 6, 11, and 16 objected to because of the following informalities: Claims 6, 11 and 16 recite a size but do not further recite a unit (e.g., bits, bytes etc.). It appears the unit is bits. Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. CLAIMS 6, 11, 16 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   CLAIMS 6, 11, and 16 recite variables N, and M without identifying what N and M represent (e.g., positive integers). The claims are therefore indefinite because it is unclear what N and M represent.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **CLAIMS 1-4, 7-9, AND 12-14** rejected under 35 U.S.C. 102(b) as being anticipated by Nogradi (US Pat no. 5974518).

   As per claim 1, Nogradi discloses a butter management system for providing a plurality of independent buffers for use by an application, the system comprising:

- a buffer memory (see FIG 2: 24 and COL 3 LINE 61: "RAM memory 24"), and
- a controller operably coupled to the buffer memory (see FIG 2: 14 and COL 3 LINE 60: "Ethernet controller 14"), the controller configured to partition the buffer memory into the plurality of independent buffers (see FIG 1 and also COL 11 43-45: "The controller 14 reconfigures the shared memory") dependent upon a partition parameter (COL 11 LINES 37-41: 'using these new values') received from the application (see FIG 2: 41) that indicates a quantity of the plurality (see COL 4 LIENS 24-30),

  [Nogradi discloses an application to provide partition parameter and a controller to divide the memory accordingly.]
- wherein each buffer of the plurality of independent butters has a buffer-size that is an integer power of two (see COL 3 LINES 63: '64 Kbytes of address space' and COL 7 LINES 1-9: 'buffers must be the same size') , to facilitate circular access to the buffer
- wherein the controller is further configured to provide (see COL 11 LINES 20-23) a write interface (see COL 11 LINE 27: "receive descriptor table") and a read interface to the application (see COL 11 LINE 28: "transmit descriptor table"),

  [The receive descriptor table allows for writing frames to the shared memory, and the transmit descriptor table allows for reading of frames from the shared memory.]

- the write interface receiving, from the application, an identification of data to be stored (see FIG 2: 'RD1') and an identification of a select buffer of the plurality of independent buffers to store the data (see COL 4 LINES 54-59) and
- translating the identification of the select buffer to an address corresponding to the select buffer (see COL 4 LINES 21-24: 'points to'), and
- the read interface receiving, from the application, the identification of the select buffer (see FIG 2: 'RD1'), and translating the identification of the select buffer to an address corresponding to the select buffer (see COL 4 LINES 21-24: 'points to').

As per claim 2, Nogradi discloses the buffer management system of claim 1,

- wherein the controller is configured to include a circular-increment function that requires only an address-increment function (see COL 6 LINE 18: "buffer index (pointer 51 in FIG 2) is incremented by one") and a bit-overwrite function to effect a circular-increment of a pointer to a select buffer of the plurality of independent buffers (see COL 4 LINES 13-15: "circular queue").

  [The index bits are overwritten as they are incremented.]

As per claim 3, Nogradi discloses the buffer management system of claim 1,

- wherein the buffer sizes of independent buffers are equal (see COL 7 LINES 1-8).

As per claim 4, Nogradi discloses the buffer management system of claim 1,

- wherein the controller is further configured to allocate the plurality of independent buffers among a plurality of independent buffers among a plurality of source-destination paths (see FIG 1: 10, 12).

  [Nogradi discloses a controller to allocate buffers for receiving and transmitting buffers for a network comprising a plurality of sources and plurality of destinations (see FIG 1: 12 and COL 3 LINES 50-53).]

As per claim 7, Nogradi discloses a method of providing a plurality of independent buffers for use by an application, the method comprising:

- receiving, at a controller, a partition parameter (COL 11 LINES 37-41: 'using these new values') from the application (see FIG 2: 41),
- partitioning a memory buffer into the plurality of independent buffers based on the partition parameter (see FIG 1 and also COL 11 43-45: "The controller 14 reconfigures the shared memory"),
- wherein a size of each buffer of the plurality of independent buffers is an integer power of two (see COL 3 LINES 63: '64 Kbytes of address space' and COL 7 LINES 1-9: 'buffers must be the same size'), thereby facilitating circular-addressing of each buffer
- providing a write-interface see COL 11 LINE 27: "receive descriptor table") that receives, from the application, an identification of data to be

stored and an identification of a select buffer of the plurality of independent buffers (see FIG 2: 'RD1' and also COL 4 LINES 54-59) to store the data,

- translating the identification of the select buffer into an address corresponding to the select buffer at which the data is to be stored buffer (see COL 4 LINES 21-24: 'points to'), and
- providing a read-interface (see COL 11 LINE 28: "transmit descriptor table"), that receives, from the application, the identification of the select buffer (see FIG 2: 'RD1' and also COL 4 LINES 54-59).

As per claim 8, Nogradi discloses the method o claim 7,

- wherein the buffer sizes of independent buffers are equal (see COL 7 LINES 1-8).

As per claim 9, Nogradi discloses the method of claim 7,

- further including providing circular- addressing for each buffer, wherein the circular-addressing includes: incrementing an address to the buffer memory (see COL 6 LINE 18: "buffer index (pointer 51 in FIG 2) is incremented by one"), and overwriting select bits of the address, corresponding to an index to the buffer within the buffer memory (see COL 4 LINES 13-15: "circular queue").

  [The index bits are overwritten as they are incremented.]

As per claim 12, Nogradi discloses an integrated circuit for providing a plurality of buffers for use by an application, the circuit comprising

- a buffer memory (see FIG 2: 24), and

- a controller that includes write control logic and read control logic (see FIG 2: 26), wherein the controller is configured to partition the buffer memory into the plurality of buffers based on a partition parameter that is provided to the controller by the application (see COL 11 39-41), each buffer of the plurality of buffers having a size that is an integer power of two (see COL 3 LINES 63: '64 Kbytes of address space' and COL 7 LINES 1-9: 'buffers must be the same size'), and
- the write control logic and read control logic are each configured to facilitate use of each buffer as a circular buffer (see COL 4 LINES 14-16).

As per claim 13, Nogradi discloses the integrated circuit of claim 12,

- wherein the buffer sizes of independent buffers are equal (see COL 7 LINES 1-8).

As per claim 14, Nogradi discloses the integrated circuit of claim 12,

- wherein the use of each buffer as a circular buffer requires circular-addressing, and the controller is configured to effect the circular-addressing via an incrementer that is configured to increment an address to the buffer memory (see COL 6 LINE 18: "buffer index (pointer 51 in FIG 2) is incremented by one"), and a bit masker that is configured to overwrite select bits of the address, corresponding to an index to the buffer within the buffer memory see COL 4 LINES 13-15: "circular queue").

  [The index bits are overwritten as they are incremented.]

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **CLAIMS 1,6,7,11,12,16** rejected under 35 U.S.C. 103(a) as being unpatentable over Shemla et al. (US Pat No. 5809557) in view of Brown et al. (US Pat No. 5916309).

As per claim 1, Shemla et al. disclose a buffer management system, comprising:

- a buffer memory (see Shemla et al. FIG 1: 12), and
- a controller (see FIG 1) operably coupled to the buffer memory, the controller configured to partition the buffer memory into the plurality of independent buffers (see Shemla et al. COL 2 LINES 54-55: "a memory array 12 (i.e., RAM) is partitioned into multiple sections),

  [The control circuitry as disclosed in FIG 1 is construed as a controller as claimed.]
- wherein each buffer of the plurality of independent buffers has a buffer-size that is an integer power of two (see Shemla et al. COL 2 LINES 66-67), to facilitate circular-access to the buffer and

- the controller is configured to provide a write-interface (see COL 3 LINES 27-31) and a read-interface to the application (see COL 3 LINES 52-55),
- an identification of a select buffer of the plurality of independent buffers to store the data (see COL 4 LINES 27-30) and
- translating the identification of the select buffer to an address corresponding to the select buffer (see COL 3 LINES 33-35), and
- the read-interface receiving, from the application, the identification of the select buffer (see COL 3 LINE 56: "RD_SEL"), and
- translating the identification of the select buffer to an address corresponding to the select buffer (see COL 3 LINES 65).

However, Shemla et al. do not expressly disclose the partitioning is

- dependent upon a partition parameter received from the application that indicates a quantity of the plurality

In the same field of endeavor, Brown et al. disclose partitioning a memory into a plurality of buffers

- dependent upon a partition parameter received from the application that indicates a quantity of the plurality (see Brown et al. ABSTRACT)

At the time of invention it would have bee obvious to a person of ordinary skill in the art to modify the circuit of Shemla et al. to determine a size of each buffer (see e.g., Shemla et al. COL 4 LINES 15-25) based on a partition parameter provided to the controller as suggested by Brown et al. (see Brown et al. COL 3 LINES 39-45).

The suggestion/motivation for doing so would have been because Brown et al. disclose the method of dynamically partitioning the memory based on a parameter improves memory utilization (see Brown et al. COL 5 LINES 28-37).

Therefore it would have been obvious at the time of invention to modify the circuit of Shemla et al. to partition the memory based on a partitioning parameter as taught by Brown et al. for the benefit of improved memory utilization to arrive at the invention as specified in the claims.

As per claims 6, Shemla et al. in view of Brown et al. disclose the buffer management system of claim 1, wherein

- the buffer memory is addressed by an M-bit address (see Shemla et al. COL 3 LINE 20: 'WR_ADDR') each buffer of the plurality of independent buffers is indexed by an N-bit index (see Shemla et al. COL 3 LINE 25: 'WR_SEL') that forms a set of N most-significant-bits of the M-bit address (see Shemla et al. COL 3 LINES 25-26: 'upper 3 bits'), and
- the size of each buffer is at least 2^{M-N} (see Shemla et al. FIG 2: 40)

As per claim 7, Shemal et al. disclose a method of providing a plurality of independent buffers for use by an application, the method comprising:

- wherein a size of each buffer of the plurality of independent buffers is an integer power of two (see Shemla et al. COL 2 LINES 66-67), thereby facilitating circular-addressing of each buffer

- providing a write-interface (see COL 3 LINES 27-31) that receives, from the application, an identification of data to be stored and an identification of a select buffer of the plurality of independent buffers to store the data (see COL 4 LINES 27-30),
- translating the identification of the select buffer into an address corresponding to the select buffer at which the data is to be stored (see COL 3 LINES 33-35), and
- providing a read-interface that receives, from the application, the identification of the select buffer (see COL 3 LINES 65).

However, Shemla et al. do not expressly disclose

- receiving, at a controller, a partition parameter from the application, partitioning a memory buffer into the plurality of independent buffers based on the partition parameter

In the same field of endeavor, Brown et al. disclose partitioning a memory into a plurality of buffers

- dependent upon a partition parameter received from the application that indicates a quantity of the plurality (see Brown et al. ABSTRACT)

At the time of invention it would have bee obvious to a person of ordinary skill in the art to modify the circuit of Shemla et al. to determine a size of each buffer (see e.g., Shemla et al. COL 4 LINES 15-25) based on a partition parameter provided to the controller as suggested by Brown et al. (see Brown et al. COL 3 LINES 39-45).

The suggestion/motivation for doing so would have been because Brown et al. disclose the method of dynamically partitioning the memory based on a parameter improves memory utilization (see Brown et al. COL 5 LINES 28-37).

Therefore it would have been obvious at the time of invention to modify the circuit of Shemla et al. to partition the memory based on a partitioning parameter as taught by Brown et al. for the benefit of improved memory utilization to arrive at the invention as specified in the claims.

As per claims 11, Shemla et al. in view of Brown et al. disclose the method of claim 7, wherein

- the buffer memory is addressed by an M-bit address (see Shemla et al. COL 3 LINE 20: 'WR_ADDR') each buffer of the plurality of independent buffers is indexed by an N-bit index (see Shemla et al. COL 3 LINE 25: 'WR_SEL') that forms a set of N most-significant-bits of the M-bit address (see Shemla et al. COL 3 LINES 25-26: 'upper 3 bits'), and
- the size of each buffer is at least 2^{M-N} (see Shemla et al. FIG 2: 40)

As per claim 12, Shemla et al. disclose an integrated circuit for providing a plurality of independent buffers for use by an application, the circuit comprising

- a buffer memory (see Shemla et al. FIG 1: 12), and

- a controller (see FIG 1) that includes write control logic and read control logic,
- wherein the controller configured to partition the buffer memory into the plurality of independent buffers (see Shemla et al. COL 2 LINES 54-55: "a memory array 12 (i.e., RAM) is partitioned into multiple sections), [The control circuitry as disclosed in FIG 1 is construed as a controller as claimed.]
- each buffer of the plurality of independent buffers has a buffer-size that is an integer power of two (see Shemla et al. COL 2 LINES 66-67), to facilitate circular-access to the buffer and
- the write control logic and read control logic are configured to facilitate use of each buffer as a circular buffer (see FIG 1: WR0, RD0), and [Shemla et al. disclose incrementing logic to address the buffer.]
- wherein the write control logic interface (see COL 3 LINES 27-31) effects a storage of a data value to a select buffer of the plurality of buffers based on an identification value of the data value and an identification of the select buffer (see COL 4 LINES 27-30) by translating the identification of the select buffer into an address corresponding to the select buffer at which the data is to be stored (see COL 3 LINES 33-35), and
- the read control logic effects retrieval of the data value based on the identification of the select buffer (see COL 3 LINE 56: "RD_SEL")

However, Shemla et al. do not expressly disclose the controller is configured to

- partition the buffer memory into the plurality of buffers based on a partition parameter that is provided to the controller by the application

  [Shemla et al. disclose partitioning the buffer into N partitions, however Shemla et al. do not expressly disclose the partitioning is based on a partition parameter provided to the controller.]

In the same field of endeavor, Brown et al. disclose partitioning a buffer

- based on a partition parameter that is provided to the controller (see Brown et al. COL 3 LINE 39-45: 'communication parameter')

Brown et al. and Shemla et al. are analogous art because they are from the same field of endeavor, namely memory access and control.

At the time of invention it would have bee obvious to a person of ordinary skill in the art to modify the circuit of Shemla et al. to partition a buffer based on a partition parameter provided to the controller as suggested by Brown et al. (see Brown et al. COL 3 LINES 39-45).

The suggestion/motivation for doing so would have been because Brown et al. disclose the method of dynamically partitioning the memory based on a parameter improves memory utilization (see Brown et al. COL 5 LINES 28-37).

Therefore it would have been obvious at the time of invention to modify the circuit of Shemla et al. to partition the memory based on a partitioning parameter as taught by Brown et al. for the benefit of improved memory utilization to arrive at the invention as specified in the claims.

As per claim 16, Shemla et al. disclose the integrated circuit of claim 12, wherein

- the buffer memory is addressed by an M-bit address (see Shemla et al. COL 3 LINE 20: 'WR_ADDR') each buffer of the plurality of independent buffers is indexed by an N-bit index (see Shemla et al. COL 3 LINE 25: 'WR_SEL') that forms a set of N most-significant-bits of the M-bit address (see Shemla et al. COL 3 LINES 25-26: 'upper 3 bits'), and
- the size of each buffer is at least 2^{M-N} (see Shemla et al. FIG 2: 40)

IV. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Applicants' arguments filed 16 January 2008 have been fully considered but they are not deemed persuasive. A response to Applicants' argument appears below.

STATUS OF REJECTIONS/OBJECTIONS

WITHDRAWN IN VIEW OF APPLICANTS AMENDMENTS/ARGUMENTS:

Objection to claims 12-16.

RESPONSE TO AMENDMENTS/ARGUMENTS

1st POINT OF ARGUMENT:

Applicants' representative argues the cited portions of Nogradi et al. do not correspond to the claimed invention because Nogradi et al. do not disclose performing a translation of the identification of the buffer received from the application to the address of the buffer in order to store the data in the buffer.

Examiner respectfully disagrees. Nogradi et al. discloses a buffer descriptor index to identify a buffer descriptor associated with the buffer. Nogradi further discloses addressing the buffer with an address of the memory.

Examiner contends a translation occurs to access the buffer because the shared memory location of the buffer cannot be addressed using a buffer descriptor index. A buffer access is initiated with a buffer descriptor index, but the location of the buffer in the shared memory cannot be accessed using the buffer descriptor index because the buffer descriptor index is separate from the shared memory address. A translation from a buffer descriptor index to a shared memory address based on the mapping in the buffer descriptor therefor occurs to perform read/write access to the buffer (see also COL 12 LINE 67-COL 13 LINE 1).

2nd POINT OF ARGUMENT:

Applicants' representative argues there is no reason to combine Shemla with Brown in the manner asserted in the previous office action.

The previous office action cited to Brown et al. COL 5 LINES 28-37 to provide motivation for modifying Shemla et al. to determine the number of partitions based on a parameter of an application that will use the buffers.

Brown et al. disclose at the cited portion:

> "A primary advantage of this method of buffer management is in its optimized memory utilization. The memory available for the port is always used in a manner that is most advantageous for the current connection parameter."

Specifically Brown et al. disclose by partitioning the memory based on a partition parameter, the memory utilization is improved.

The previous office action further stated, in response to the arguments that Shemla et al. could not support the feature of "dynamically partitioning the memory," that the claims do not recite dynamically partitioning the memory.

Brown et al. was *only* relied upon to teach determining a number of partitions based on a communication parameter acquired from the application that will use the buffers.

Examiner contends it would have been obvious to a person of ordinary skill in the art to determine the number of partitions based on a communication parameter acquired from the application that will use the buffers as suggested by Brown et al. to arrive at the invention as specified in the claims.

V. CLOSING COMMENTS

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

Va. CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-4, 6-9, 11-14 and 16 have received a third action on the merits and are subject of a non office action.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

VI. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kalpit Parikh/

13 April 2008

Kalpit Parikh
Examiner
Art Unit 2187

/Brian R. Peugh/
Primary Examiner, Art Unit 2187
4/18/08